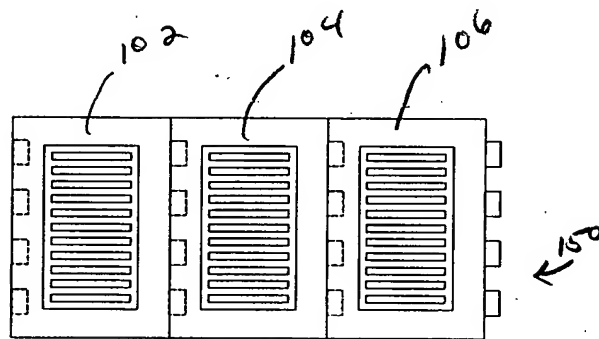


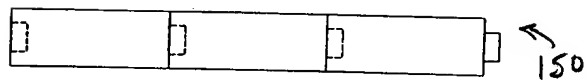
Individual Cells

FIG. 1A



Cells Assembled into Array

FIG. 1B



Edge View of Assembled Array

FIG. 1C

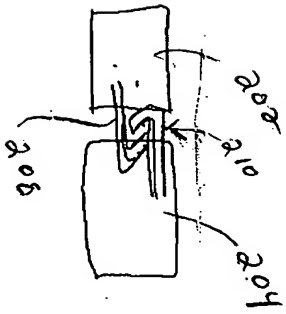


FIG. 2A

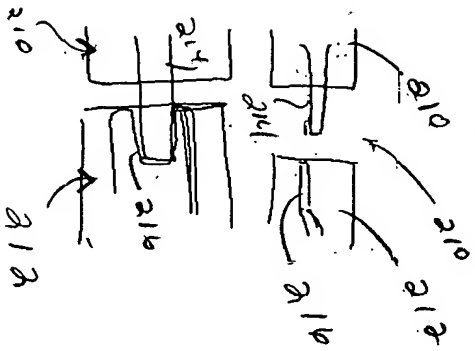


FIG. 2B

FIG. 2C

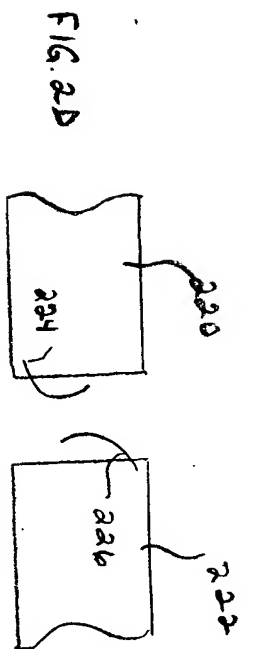


FIG. 2D

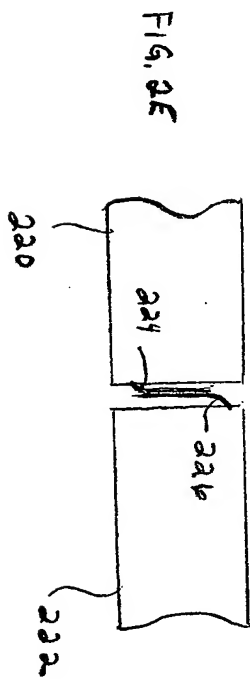


FIG. 2E

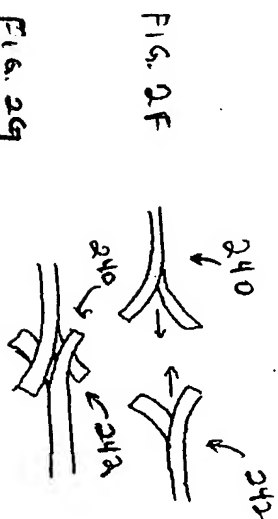


FIG. 2F

FIG. 2G

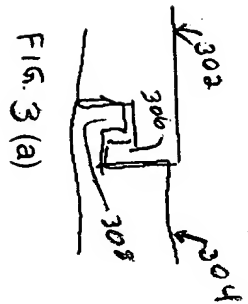


FIG. 3(a)

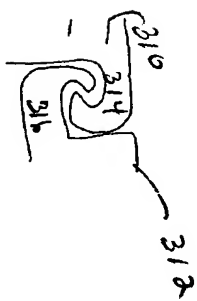


FIG. 3(b)

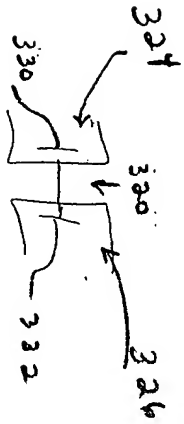


FIG. 3(c)

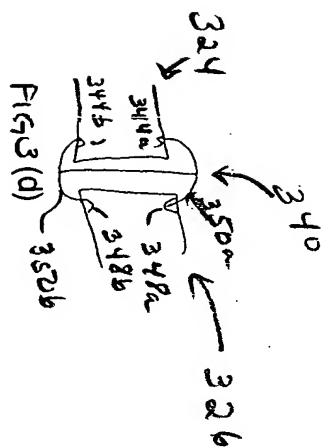


FIG. 3(d)

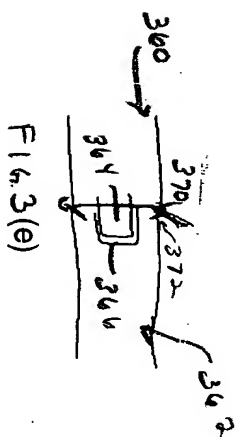


FIG. 3(e)

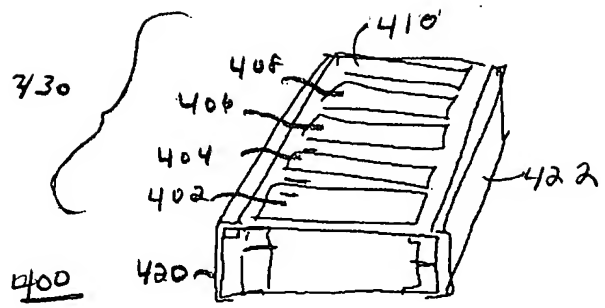


Figure 4: Edge Bracket

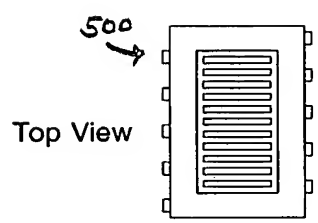


FIG. 5A

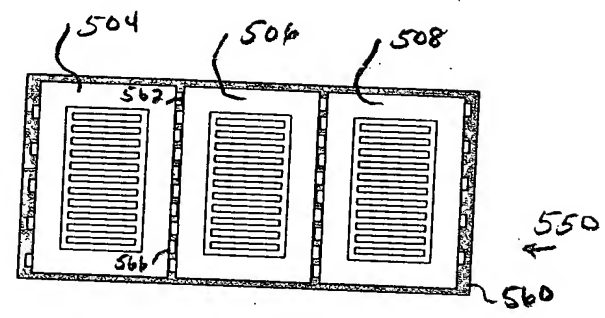


FIG. 5B

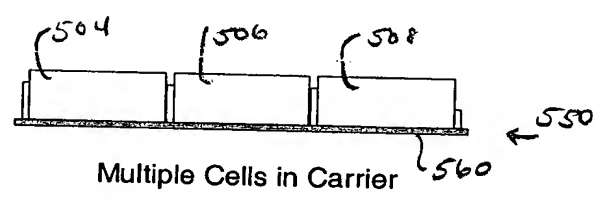


FIG. 5C

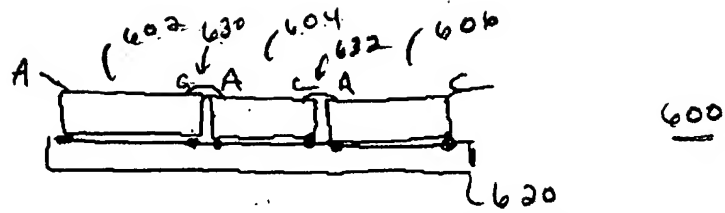


Figure 6: Carrier method with electrical connections between cells

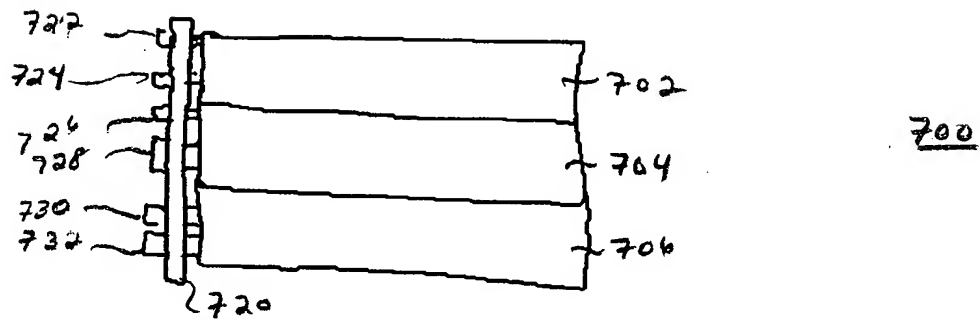


Figure 7: Carrier method with side-located circuit board